Serial No. : New National Stage Application
Filed : PCT Filing Date; December 26, 2003

REMARKS

This preliminary amendment is made for the above-identified case which is a national stage application based on International Application No. PCT/JP03/16900. In the amendment, Applicant has corrected the forms of the original claims to remove the multiple dependency forms of the claims. Applicant respectfully requests the entrance of the amendment before substantive examination of this case.

Respectfully submitted,

MURAMATSU & ASSOCIATES

Dated: 9/7/04 By: [signature]

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ABSTRACT

A recovery clock synchronized with an internal clock faster than a system clock is obtained with an edge timing of the system clock output from a DUT. The present invention is configured to comprise: a time interpolator 20 which includes flip-flops 21a to 21n which receive system clocks of the DUT 1, a delay circuit 22 which sequentially receives strobes delayed at specified timing intervals to the FF 21 and outputs time-series level data, and an encoder 28 which receives the time-series level data output from the FF 21 and encodes it into positional data indicative of an edge timing; a digital filter 40 which includes a plurality of registers 41a to 41n which sequentially store the positional data of the encoder 28 and output it with a predetermined timing, and outputs the positional data from the register 41 as a recovery clock; and a data side selector 30 which selects output data of the DUT 1 with the recovery clock being used as a selection signal.